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(54) Electronic delay circuit for firing ignition element.

(57) An electronic delay circuit for firing an ignition element (18). The delay circuit includes a capacitor (15) which stores electric energy supplied from an electric blasting machine (1), an oscillator (92) generating a clock pulse train, a circuit (70) for over-exciting the oscillator, a counter (50) which counts clock pulses of the clock pulse train, and a circuit (40) for maintaining a reset state of the counter for a predetermined time period after the electric energy is supplied. The counter (50) produces a trigger signal when it counts a predetermined number of the clock pulses, and the electric energy stored in the capacitor (15) is discharged to the ignition element (18). Since the oscillator (92) enters into the steady state in a very short time by the over-excitation, the delay circuit has large resistance to external noise.

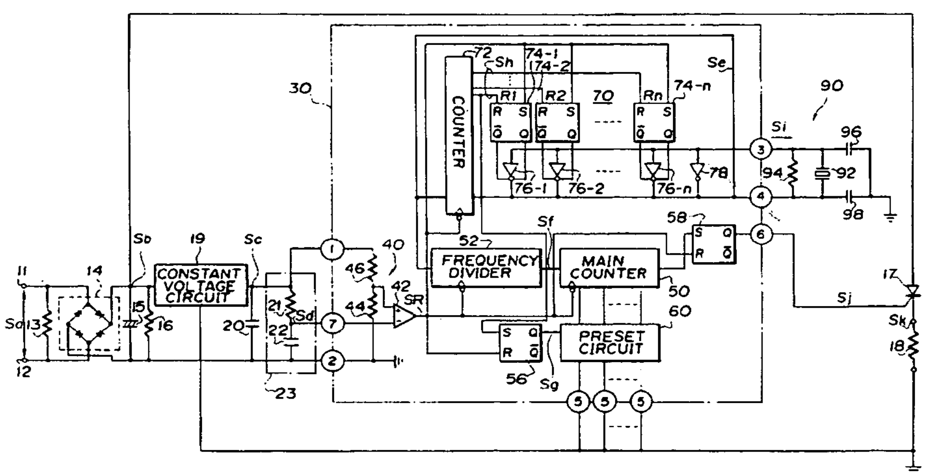

FIG.3

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The present invention relates to an electronic delay circuit for firing an ignition element, which stores electric energy supplied from an electric blasting machine, and fires at high accuracy a detonator following a predetermined delay.

A method for controlling ground vibrations so as to minimize the effect of blasting on nearby structures in a multi-step blasting system is proposed by Japanese Patent Application Laying-open No. 285800/1989. This application teaches the accuracy of a delay time interval for sequentially firing detonators in order to reduce the ground vibrations. According to the application, it is preferable that the delay time interval t and the standard deviation σ of the delay time interval t satisfy the following relationship:

$t/\sigma \geqq 10$ (1).

The application states that unless the condition is satisfied, the ground vibrations may not be reduced.

Consequently, in order to set the delay time interval for firing detonators at 10 ms, the standard deviation of the delay time must be equal or less than 1 ms. Likewise, the delay time interval of 5 ms requires the standard deviation of 0.5 ms or less.

Japanese Patent Application Publication No. 53479/1988 discloses an electric detonator fired by an electronic delay circuit. This circuit receives only electric energy via leading wires, activates a digital timer comprising a quartz or ceramic oscillator, and fires an electric detonator after a predetermined delay time. The application, however, does not teaches a technique to satisfy the condition of equation (1).

U. S. Patent No. 4,445,435 teaches an electronic delay blasting circuit which comprises a means for storing electric energy, an oscillating circuit using a quartz or ceramic oscillator, a digital timer including a counter and a counter reset circuit for resetting the counter, and a means for firing an electric detonator after a predetermined delay time.

Likewise, European Patent Application Publication No. 261,886 discloses a delay circuit for electrically firing a detonating primer (detonator).

Figs. 1 and 2 illustrate the principle of a delay circuit disclosed by the European patent application. In this figure, an electric blaster (electric blasting machine) 1 supplies a voltage (electric energy) as shown at (a) of Fig. 2. The electric energy is supplied to an actuation circuit 2, a capacitor 3, a clock pulse generator 4 and a counting circuit 5 via leading wires 6, and is stored into the capacitor 3 as shown at (b) of Fig. 2. The actuation circuit 2 maintains the reset state of the counting circuit 5 during counter reset time T (= 200 - 300 ms), and actuates the counting circuit 5 to start counting when the counter reset time T has elapsed after the application of the input voltage is initiated. The time T is defined by the falling edge of the input voltage as shown at (a) and (c) of Fig. 2. This is because the output frequency of a quartz or ceramic oscillator included in the clock pulse generator 4 becomes stable after the counter reset time T as shown at (c) of Fig. 2. The counting circuit 5 counts the pulses of the pulse train produced by the clock pulse generator 4, and trigger a switching circuit 7 as shown at (d) of Fig. 2, so that a current is supplied from the capacitor 3 to an ignition circuit 8. Thus, an electric detonating primer (detonator) is fired after a predetermined delay time as shown at (e) of Fig. 2.

The quartz or ceramic oscillator employed by the clock pulse generator 4 has a problem in that the oscillator takes approximately 200 - 300 ms before it enters into a steady state oscillation. In other words, the output frequency thereof is unstable during the counter reset time T. Accordingly, the prior art cannot start counting pulses of the pulse train outputted from the oscillator until the counter reset time T has elapsed.

The long counter reset time T presents a problem in that the delay time becomes unstable. There are two major reasons for this.

First, as the counter reset time increases, the probability that the input voltage as shown at (a) of Fig. 2 may be influenced by external noise during the counter reset time T increases. The external noise may change the falling edge of the input voltage, and hence will change the starting time of the counting circuit 5. This is a great problem because there is much noise caused by incomplete contact of the lines (leading wires) or by switching the electric blasting machine or the like in a blasting site. To improve such a problem, the actuation circuit 2 becomes complicated, and hence increase in size and cost thereof will be unavoidable.

Second, as the counter reset time increases, the error of the counter reset time will increase since the counter reset time is specified by the analog voltage. In addition, the increasing electric power will be consumed as the counter reset time becomes longer.

In addition, it is difficult to apply the prior art to a serially connected blasting system.

It is therefore an object of the present invention to provide an electronic delay circuit for firing an ignition element that can improve the accuracy of delay time for firing a detonator.

It is another object of the present invention to provide an electronic delay circuit for firing an ignition element that can reduce the electric power consumed during the operation of a timer circuit.

In a first aspect of the present invention, there is provided an electronic delay circuit for firing an ignition element comprising:

means for storing electric energy supplied from an electric blasting machine;

means for oscillating a clock pulse train by using the electric energy stored in the means for storing;

means for over-exciting the means for oscillating;

means for counting clock pulses of the clock pulse train;

means for producing a trigger signal when the means for counting counts a predetermined number of the clock pulses of the clock pulse train; and

means for discharging electric energy stored in the means for storing to the ignition element in response to the trigger signal.

The means for over-exciting may comprise means for supplying current from the means for storing to the means for oscillating for a first predetermined time after the electric energy is supplied.

An electronic delay circuit for firing an ignition element may further comprise means for maintaining a reset state of the means for counting for a second predetermined time period after the electric energy is supplied, wherein the means for maintaining a reset state may release the reset state when the second predetermined time period is over so that the means for counting starts counting.

The means for maintaining the reset state may comprise a time constant circuit and a comparator, the time constant circuit comprising a capacitor and a resistor, and the comparator comparing a voltage across the capacitor with a predetermined reference voltage.

The second predetermined time period of the means for maintaining the reset state may be equal to or less than 5 ms.

An electronic delay circuit for firing an ignition element may further comprise discharging means, connected in parallel with the means for storing, for promoting discharge of the electric energy stored in the means for storing.

The means for counting may be a preset counter whose initial value is set by cutting preset wire.

An electronic delay circuit for firing an ignition element may further comprise means for presetting the initial value of the preset counter, wherein the means for presetting may comprise means for disconnecting the means for presetting from the means for storing after the preset of the initial value has been completed.

An electronic delay circuit for firing an ignition element may further comprise a resistor connected between lines carrying the electric energy inputted to the means for storing.

The means for oscillating, means for counting, and means for over-exciting may be integrated into one IC chip.

In a second aspect of the present invention, there is provided an electronic delay circuit for firing an ignition element comprising:

means for storing electric energy supplied from an electric blasting machine;

means for oscillating a clock pulse train by using the electric energy stored in the means for storing;

means for maintaining a reset state of the means for counting for a second predetermined time period after the electric energy is supplied, by using the electric energy stored in the means for storing, the means for maintaining a reset state releasing the reset state when the second predetermined time period is over so that the means for counting starts counting;

means for producing a trigger signal when the means for counting counts a predetermined number of the clock pulses of the clock pulse train; and

means for discharging electric energy stored in the means for storing to the ignition element in response to the trigger signal.

According to the present invention, the output frequency of the means for oscillating reaches a steady state frequency in a very short time because of the over-excitation. As a result, the accuracy of the delay time for firing the detonator is improved. In addition, since the means for counting starts counting after the output frequency has entered into the steady state, a high precision, reliable delay time can be obtained.

Furthermore, the short rising time of the oscillation reduces the power consumption of the oscillator. As a result, the size of the capacitor storing the electric energy can be reduced. This makes it possible to provide easy-to-use detonators.

In the present invention, the counter reset time is created inside the delay circuit. Therefore, detection of the external signal for controlling the counter reset time is unnecessary unlike the prior art stated before. Thus, a highly reliable electronic detonator can be achieved.

The counter reset time is set at approximately equal to the time during which the output frequency of the means for oscillating reaches the steady state. Since the counter reset time is very short in the present invention, a simple circuit comprising the capacitor and the resistor can achieve a sufficiently accurate counter reset time. This reduces the cost of the circuit.

The above and other objects, effects, features and advantages of the present invention will become more apparent from the following description of the embodiment thereof taken in conjunction

with the accompanying drawings.

Fig. 1 is a schematic block diagram illustrating a principle of a prior art electronic delay circuit for use in a detonator;

Fig. 2 is a diagram illustrating waveforms of various portions of Fig. 1;

Fig. 3 is a block diagram showing an embodiment of an electronic delay circuit for firing an ignition element in accordance with the present invention;

Fig. 4A is a circuit diagram showing a preset circuit of Fig. 3;

Fig. 4B is a circuit diagram showing a clocked inverter of Fig. 3;

Fig. 5 is a diagram illustrating waveforms of various portions of Fig. 3;

Figs. 6A and 6B are diagrams comparatively illustrating waveforms of the embodiment shown in Fig. 3 and the prior art shown in Fig. 1;

Fig. 7 is a longitudinal sectional view of a detonator in accordance with the present invention; and

Figs. 8A and 8B are diagrams showing an arrangement of components packed in the detonator.

The invention will now be described with reference to the accompanying drawings.

Fig. 3 is a block diagram showing an embodiment in accordance with the present invention.

In this figure, input terminals 11 and 12 are connected to the electric blasting machine 1 of Fig. 1 via leading wires 6. A resistor 13 and a rectifier 14 are connected between the input terminals 11 and 12. A capacitor 15 and a resistor 16 are connected in parallel between the output terminals of the rectifier 14. The resistor 13 prevents stray current, which may often take place in a blasting site, from charging the capacitor 15 to such a voltage as firing the detonator. Furthermore, the resistor 13 serves as a voltage divider when a plurality of detonators are connected in series in a multi-step blasting system so that an approximately equal voltage is supplied to each rectifier 14. The rectifier 14 makes it possible for the capacitor 15 to be charged in one direction regardless of the polarity of the input voltage supplied to the terminals 11 and 13. In this embodiment, the resistance of the resistor 13 is 15 Ω, and the capacitor of the capacitance 15 is 1,000 microfarad. In this case, the capacitor 15 is charged to the maximum voltage of 15 V in 5 - 10 ms by the electric energy supplied from the electric blasting machine 1.

A serial circuit of a thyristor (a switching device) 17 and an igniting resistor 18 is connected across the capacitor 15. In addition, the input terminals of a constant voltage circuit 19 are connected across the capacitor 15. A capacitor 20 and a serial circuit of a resistor 21 and a capacitor 22 are connected in parallel across the output terminals of the constant voltage circuit 19. The resistor 21 and the capacitor 22 constitute a counter reset time circuit 23. Further, a digital timer 30 is connected to the output terminals of the constant voltage circuit 19.

The digital timer 30 comprises a reset circuit 40, a main counter 50 that counts the delay time for firing the detonator, a preset circuit 60 that presets an initial value of the main counter 50, a over-exciting circuit 70 for over-exciting an oscillator 90 so that the oscillator 90 enters into steady state in a very short time.

The reset circuit 40 comprises a comparator 42, and a voltage divider consisting of resistors 44 and 46. The inverting input terminal of the comparator 42 is connected to the connecting point of the resistor 21 and the capacitor 22, and the noninverting input terminal of the comparator 42 is connected to the connecting point of the resistors 44 and 46. Accordingly, the output of the comparator 42 changes from a high level to a low level after a predetermined time T1 defined by the time constant of the resistor 21 and the capacitor 22. The predetermined time T1 is specified as 5 ms, for example, which corresponds to the counter reset time of the present invention.

The main counter 50 is a 13-bit preset type counter to which a pulse train Sf is supplied from a frequency divider 52. The frequency divider 52 is a 12-bit divider. Thus, the output frequency of the divider 52 is 1/4096 of the frequency of the clock pulse train Se supplied from the oscillator 90.

The main counter 50 is connected to the preset circuit 60 which presets the initial value of the main counter 50. The preset circuit 60 is activated by a flip-flop 56. The flip-flop 56 is reset by the rising edge of the signal SR. The main counter 50 and the frequency divider 52, on the other hand, are reset by the falling edge of the signal SR.

Fig. 4A shows the preset circuit 60 comprising a plurality of switching circuits 62. Each switching circuit 62 comprises a p-channel FET 64 and an n-channel FET 66 connected in series via a resistor 67. The gates of the two FETs are connected to the Q output of the flip-flop 56. When the flip-flop 56 is in the set state, that is, when the gate voltage is higher than a threshold voltage, the p-channel FET 64 is cut off and the n-channel FET 66 is conducted. Therefore, the output level of each switching circuit 62 is low, and preset value of the main counter 50 is unchanged. In contrast, when the flip-flop 56 is in the reset state, that is, when the gate voltage is lower the threshold voltage, the p-channel FET 64 is conducted and the n-channel FET 66 is cut off. In this case, the output level of each switching circuit 62 is determined by the state of time set lines 68-1, 68-2, ..., 68-m. The output

level of the switching circuit 62 will be low when the time set line 68-j is grounded, whereas it will be high when the time set line 68-j is open.

Referring again to Fig. 3, the output of the main counter 50 is supplied to a flip-flop 58, and sets the flip-flop 58 which has been previously reset by the rising edge of the signal SR. When the flip-flop 58 is set, the thyristor 17 is triggered and is turned on. Thus, all the electric energy which remains in the capacitor 15 after the delay circuit has consumed is supplied to the ignition resister 18, and the detonator explodes.

The over-exciting circuit 70 comprises an auxiliary counter 72, flip-flops 74-1, 74-2, ..., 74-n, clocked inverters 76-1, 76-2, ..., 76-n and an inverter 78. The counter 72 outputs signals R1, R2, ..., Rn every 1 µs interval, and supplies them to the reset terminal of the flip-flops 74-1, 74-2, ..., 74-n, respectively. The flip-flops 74-1, 74-2, ..., 74-n are simultaneously set by the rising edge of the signal SR, and are reset sequentially by the signals R1, R2, ..., Rn. The output terminal of the flip-flop 74-i (i = 1, 2, ..., n) is connected to the control terminal of the clocked inverter 76-i. The over-exciting circuit itself is known in the field of electronic circuit as disclosed in Fig. 9 of Japanese Patent Application Laying-open No. 200009/1992.

Fig. 4B is a circuit diagram of the clocked inverter 76-i. The control terminals 83 and 84 of the clocked inverter 76-i are connected to the output terminals of the flip-flop 74-i. The input terminal 81 and the output terminal 82 of the clocked inverter 76-i is connected to the oscillator 90. When a high level signal is applied to the control terminal 83 and a low level signal is applied to the control terminal 84, the clocked inverter functions as an inverter. On the other hand, when the low level signal is applied to the control terminal 83 and a high level signal is applied to the control terminal 84, the clocked inverter is electrically separated from the oscillator 90.

The oscillator 90 comprises a quartz oscillator 92, a feedback resistor 94 connected in parallel with the quartz oscillator 92, capacitors 96 and 98 connected between the quartz oscillator 92 and the ground. The frequency of the quartz oscillator is preferably in the range from 1 MHz to 16 MHz. If the frequency is too low, the rising time of the oscillation becomes long. As a result, the counter reset time T1 increases, and the accuracy of the delay time is adversely affected. If the frequency is too high, the power consumption increases. As a result, the capacitor 15 cannot supply enough electric energy to explode the detonator.

Next, the operation of the delay circuit of Fig. 3 will be described with reference to Fig. 5.

Fig. 5 illustrates waveforms of various portions of the delay circuit.

A voltage Sa is applied to the input terminals 11 and 12 from the electric blasting machine 1 at time t0. The electric energy provided by the voltage Sa is stored into the capacitor 15, and the voltage Sb across the capacitor 15 increases rapidly. The constant voltage circuit 19 starts operating at time t1 immediately (a few microseconds) after the application of the voltage Sa, and outputs a constant voltage Sc (= 3.3 V, for example).

The output voltage Sc is applied to the capacitor 22 through the resistor 21, and hence the voltage Sd across the capacitor 22 gradually increases. When the voltage Sd exceeds the voltage determined by the voltage divider consisting of the resistors 44 and 46 at time t2, the output of the comparator 42 changes its output level from high to low, and this change makes the falling edge of the signal SR. Thus, the falling edge of the signal SR is produced when time interval T1 (approximately 5ms in this embodiment) has elapsed after time t1. The signal SR sets the flip-flops 74-1 - 74-n, and resets the flip-flops 56 and 58 by its rising edge at time t1. On the other hand, the signal SR resets the main counter 50, the frequency divider 52, and the counter 72 by its falling edge at time t2.

During time interval T1, the quartz oscillator 92 is over-excited by the clocked inverters 76-1 - 76-n and the inverter 78, and enters into the steady state. That is, the frequency of the pulse train outputted from the quartz oscillator 92 becomes stable during the time interval T1.

At time t2, the frequency divider 52 starts its operation and outputs a pulse train Sf consisting of pulses whose interval is 1 ms. At the same time, the counter 72 starts counting of the clock pulse supplied from the oscillator 90, and generates signals R1 - Rn every 1 µs interval. The signal R1 sets the flip-flop 56 and reset the flip-flop 74-1 at time t3 which is 1 µs after time t2. Accordingly, the signal Sg applied to the preset circuit 60 rises at time t3, and separates the preset circuit 60 from the constant voltage circuit 19. This reduces the power consumed by the delay circuit.

After time t3, the flip-flops 74-1 - 74-n are sequentially reset every T2 interval (1 µs) by the signal Sh (= R1, R2, ..., Rn). Accordingly, the clocked inverters 76-1 - 76-n are sequentially cut off from the oscillator 90. Thus, the over-excitation of the oscillator 90 is gradually released by the signal Sh. As a result, the current Si supplied to the oscillator 90 gradually changes from 20 mA, which is initially supplied from the clocked inverters 76 and the inverter 78 during the over-excitation, to 0.2 mA, which is supplied by the inverter 78 during the steady state excitation.

The quartz oscillator 92 consumes substantially large power at the initial stage of oscillation, and

automatically reduces its consumption power as the oscillation approaches the steady state. Accordingly, the over-excitation of the quartz oscillator 92 by the clocked inverters, which are activated by a constant voltage, does not cause thermal damage of the oscillator, and leads the oscillation to the steady state in a very short time.

By using this feature of the quartz oscillator, the clocked inverters 76 and the inverter 78 may be replaced with an inverter that can supply sufficient current to induce the over-excitation of the quartz oscillator. In this case, the clocked inverters 76 and the flip-flops 74 can be omitted.

When the count value of the main counter 50 reaches the preset value, the main counter 50 sets the flip-flop 58. This produces a trigger signal Sj of the thyristor 17, and the current Sk is supplied from the capacitor 15 to the ignition resistor 18. Thus, the detonator explodes.

Figs. 6A and 6B are diagrams comparatively illustrating the characteristics of the present invention and the prior art described before.

The counter reset time T1 of the present invention is much shorter than that of the prior art. For example, the counter reset time T1 of the present invention is about 5 ms, whereas that of the prior art is about 200 - 300 ms. Furthermore, although the counter 50 of the present invention is started by the signal SR generated inside the circuit, the counter of the prior art is started by the input voltage supplied from the electric blasting machine 1 via the leading wires 6. As a result, the start of the counter of the prior art is susceptible to external noise. In contrast, the start of the counter of the present invention is insusceptible to external noise.

The electronic delay detonator can be miniaturized by using an IC (integrated circuit) technique.

Figs. 7, 8A and 8B illustrate the arrangement inside a detonator in accordance with the embodiment.

A cylindrical housing 144 comprises the delay circuit 100 and a shell 160. The shell 160 comprises the ignition resistor 18, ignition charge 146, space 145, primer charge 149, base charge 150. The delay circuit 100 is arranged on a printed board 147, and the output of the delay circuit 100 is applied to the ignition resistor 18 through lead wires. The printed board 147 has thereon the digital timer 30 which is integrated into an IC chip, resistors 13a and 13b constituting the resistor 13, the rectifier 14, the thyristor 17, the constant voltage circuit 19, the capacitor 22, and the oscillator 92. The capacitor 15 for storing the electric energy is attached to the printed board 147. The quartz oscillator 92 is stuck to the printed board 147 with a double adhesive tape 148. Further, the time set lines 68 are formed on the bottom side of the printed board 147. The housing is closed with a cap 151, and leg lines 152 and 153 are led from inside to outside of the housing through the cap 151.

According to this arrangement, these components can be packed into the housing 144 whose outer diameter is equal to or less than 17 mm and whose length is equal to or less than 110 mm or less. In this case, the capacitor 15 has an outer diameter equal to or less than 11 mm and a length equal to or less than 53 mm.

In this embodiment, the capacitor 22 of 6.2 μF ± 5%, and the resistor 21 of 750 kΩ ± 2% are employed. In addition, the threshold voltages of the reset terminals in the digital timer 30 are 2.07 V ± 5%. The total error caused by these errors is estimated by the mean square. The estimated total error of the counter reset time T1 is 7.9 % or ± 0.4 ms. The timer reset times T1 are measured with regard to 500 samples fabricated as test detonators, and they are within 4.7 ± 0.2 ms.

The accuracy of the quartz oscillator 92 is 30 ppm. Accordingly, when the delay time is set at 8 seconds, the error due to the quartz oscillator 92 is approximately 0.2 ms. In the case where the total error of the counter reset time T1 is 0.4 ms, the total error becomes 0.6 ms (= 0.2 + 0.4). Hence, the accuracy better than ± 1ms can be achieved.

According to the embodiment, since the counter reset time T1 is much shorter than that of the prior art, high accuracy is not required of the resistor 21 and the capacitor 22. Therefore, an inexpensive counter reset time circuit 23 can be constructed using a cheap resistor and capacitor.

In addition, low power consumption is achieved. This is because the delay circuit is composed of C-MOS ICs, and the preset circuit 60 is disconnected after the preset operation.

The digital timer 30 before packaging, to which no lead frame is attached, may be employed instead of the packaged IC digital timer. In this case, the size of the delay circuit will be further reduced. The oscillator 92 may be replaced by a chip-type oscillator which is thinner than the oscillator 92 shown in Fig. 8A.

Furthermore, all the components except for capacitors 15, 20, 22, 96 and 98 can be integrated into one IC chip. This will further miniaturize the delay circuit. Moreover, the IC chip may be contained in the shell 160.

In addition, the delay circuit 100 may be packed in a case, and may be connected to the shell 160 through a connector.

The present invention has been described in detail with respect to various embodiments, and it will now be apparent from the foregoing to those skilled in the art that changes and modifications may be made without departing from the invention in its broader aspects, and it is the intention, there-

fore, in the appended claims to cover all such changes and modifications as fall within the true spirit of the invention.

Claims

1. An electronic delay circuit for firing an ignition element characterized by comprising:
means for storing electric energy supplied from an electric blasting machine;
means for oscillating a clock pulse train by using the electric energy stored in said means for storing;
means for over-exciting said means for oscillating;
means for counting clock pulses of said clock pulse train;
means for producing a trigger signal when said means for counting counts a predetermined number of said clock pulses of said clock pulse train; and
means for discharging electric energy stored in said means for storing to said ignition element in response to said trigger signal.

2. An electronic delay circuit for firing an ignition element as claimed in claim 1, characterized in that said means for over-exciting comprises means for supplying current from said means for storing to said means for oscillating for a first predetermined time after the electric energy is supplied.

3. An electronic delay circuit for firing an ignition element as claimed in claim 1, further characterized by comprising means for maintaining a reset state of said means for counting for a second predetermined time period after the electric energy is supplied, characterized in that said means for maintaining a reset state releases said reset state when said second predetermined time period is over so that said means for counting starts counting.

4. An electronic delay circuit for firing an ignition element as claimed in claim 3, characterized in that said means for maintaining the reset state comprises a time constant circuit and a comparator, said time constant circuit comprising a capacitor and a resistor, and said comparator comparing a voltage across said capacitor with a predetermined reference voltage.

5. An electronic delay circuit for firing an ignition element as claimed in claim 3, characterized in that said second predetermined time period of said means for maintaining the reset state is equal to or less than 5 ms.

6. An electronic delay circuit for firing an ignition element as claimed in claim 1, further characterized by comprising discharging means, connected in parallel with said means for storing, for promoting discharge of said electric energy stored in said means for storing.

7. An electronic delay circuit for firing an ignition element as claimed in claim 3, further characterized by comprising discharging means, connected in parallel with said means for storing, for promoting discharge of said electric energy stored in said means for storing.

8. An electronic delay circuit for firing an ignition element as claimed in claim 1, characterized in that said means for counting is a preset counter whose initial value is set by cutting preset wire.

9. An electronic delay circuit for firing an ignition element as claimed in claim 3, characterized in that said means for counting is a preset counter whose initial value is set by cutting preset wire.

10. An electronic delay circuit for firing an ignition element as claimed in claim 8, further characterized by comprising means for presetting the initial value of said preset counter, characterized in that said means for presetting comprises means for disconnecting said means for presetting from said means for storing after the preset of the initial value has been completed.

11. An electronic delay circuit for firing an ignition element as claimed in claim 9, further characterized by comprising means for presetting the initial value of said preset counter, characterized in that said means for presetting comprises means for disconnecting said means for presetting from said means for storing after the preset of the initial value has been completed.

12. An electronic delay circuit for firing an ignition element as claimed in claim 1, further characterized by comprising a resistor connected between lines carrying said electric energy inputted to said means for storing.

13. An electronic delay circuit for firing an ignition element as claimed in claim 3, further characterized by comprising a resistor connected between lines carrying said electric energy inputted to said means for storing.

14. An electronic delay circuit for firing an ignition element as claimed in claim 1, characterized in that said means for oscillating, means for counting, and means for over-exciting are integrated into one IC chip.

15. An electronic delay circuit for firing an ignition element as claimed in claim 3, characterized in that said means for oscillating, means for counting, means for over-exciting and means for maintaining the reset state are integrated into one IC chip.

16. An electronic delay circuit for firing an ignition element characterized by comprising:

means for storing electric energy supplied from an electric blasting machine;

means for oscillating a clock pulse train by using the electric energy stored in said means for storing;

means for maintaining a reset state of said means for counting for a second predetermined time period after the electric energy is supplied, by using the electric energy stored in said means for storing, said means for maintaining a reset state releasing said reset state when said second predetermined time period is over so that said means for counting starts counting;

means for producing a trigger signal when said means for counting counts a predetermined number of said clock pulses of said clock pulse train; and

means for discharging electric energy stored in said means for storing to said ignition element in response to said trigger signal.

17. An electronic delay circuit for firing an ignition element as claimed in claim 16, further characterized by comprising means for over-exciting said means for oscillating, characterized in that said means for over-exciting comprises means for supplying current from said means for storing to said means for oscillating for a first predetermined time after the electric energy is supplied.

18. An electronic delay circuit for firing an ignition element as claimed in claim 17, characterized in that said means for maintaining the reset state comprises a time constant circuit and a comparator, said time constant circuit comprising a capacitor and a resistor, and said comparator comparing a voltage across said capacitor with a predetermined reference voltage.

19. An electronic delay circuit for firing an ignition element as claimed in claim 18, characterized in that said second predetermined time period of said means for maintaining the reset state is equal to or less than 5 ms.

20. An electronic delay circuit for firing an ignition element as claimed in claim 19, further characterized by comprising discharging means, connected in parallel with said means for storing, for promoting discharge of said electric energy stored in said means for storing.

21. An electronic delay circuit for firing an ignition element as claimed in claim 20, characterized in that said means for counting is a preset counter whose initial value is set by cutting preset wire.

22. An electronic delay circuit for firing an ignition element as claimed in claim 21, further characterized by comprising means for presetting the initial value of said preset counter, characterized in that said means for presetting comprises means for disconnecting said means for presetting from said means for storing after the preset of the initial value has been completed.

23. An electronic delay circuit for firing an ignition element as claimed in claim 22, further characterized by comprising a resistor connected between lines carrying said electric energy inputted to said means for storing.

24. An electronic delay circuit for firing an ignition element as claimed in claim 23, characterized in that said means for oscillating, means for counting, means for over-exciting and means for maintaining the reset state are integrated into one IC chip.

25. A detonator comprising an electric delay circuit and a shell contained separately into a case, said shell containing a charge, said electric delay circuit characterized by comprising:

means for storing electric energy supplied from an electric blasting machine;

means for oscillating a clock pulse train by using the electric energy stored in said means for storing;

means for maintaining a reset state of said means for counting for a second predetermined time period after the electric energy is supplied, by using the electric energy stored in said means for storing, said means for maintaining a reset state releasing said reset state when said second predetermined time period is over so that said means for counting starts counting;

means for producing a trigger signal when said means for counting counts a predetermined number of said clock pulses of said clock pulse train; and

means for discharging electric energy stored in said means for storing to said ignition element in response to said trigger signal.

26. A detonator as claimed in claim 25, characterized in that said shell comprises an ignition resistor to which an output of said delay circuit is applied.

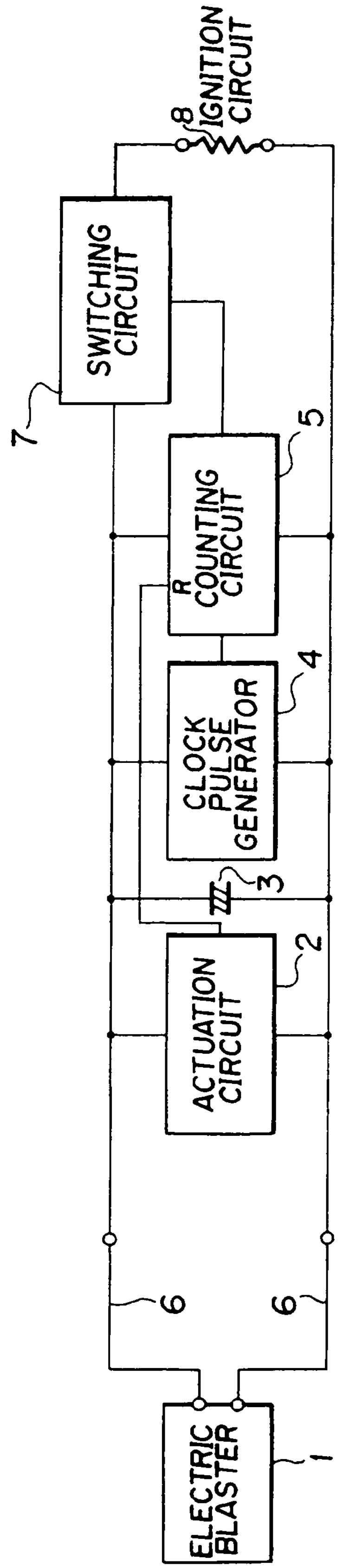

FIG.1 PRIOR ART

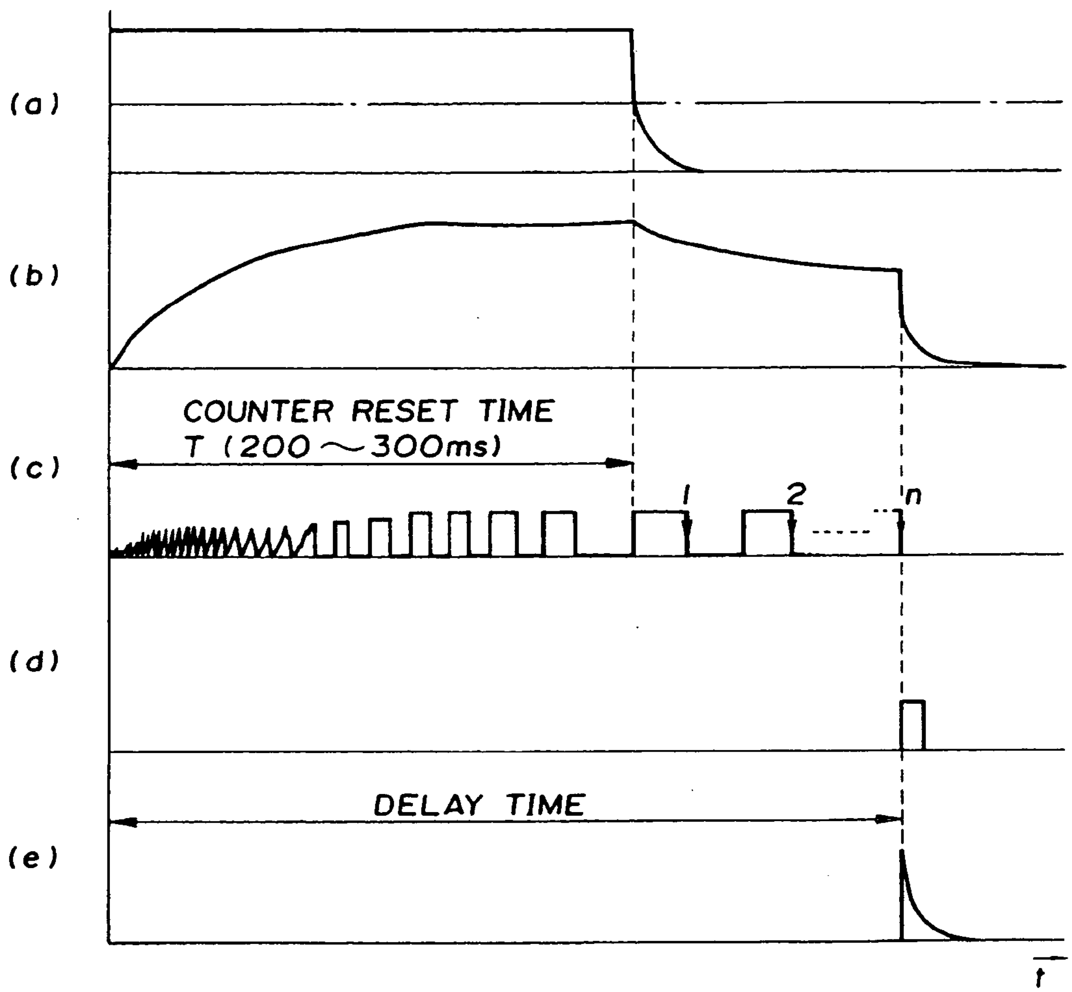

FIG.2 PRIOR ART

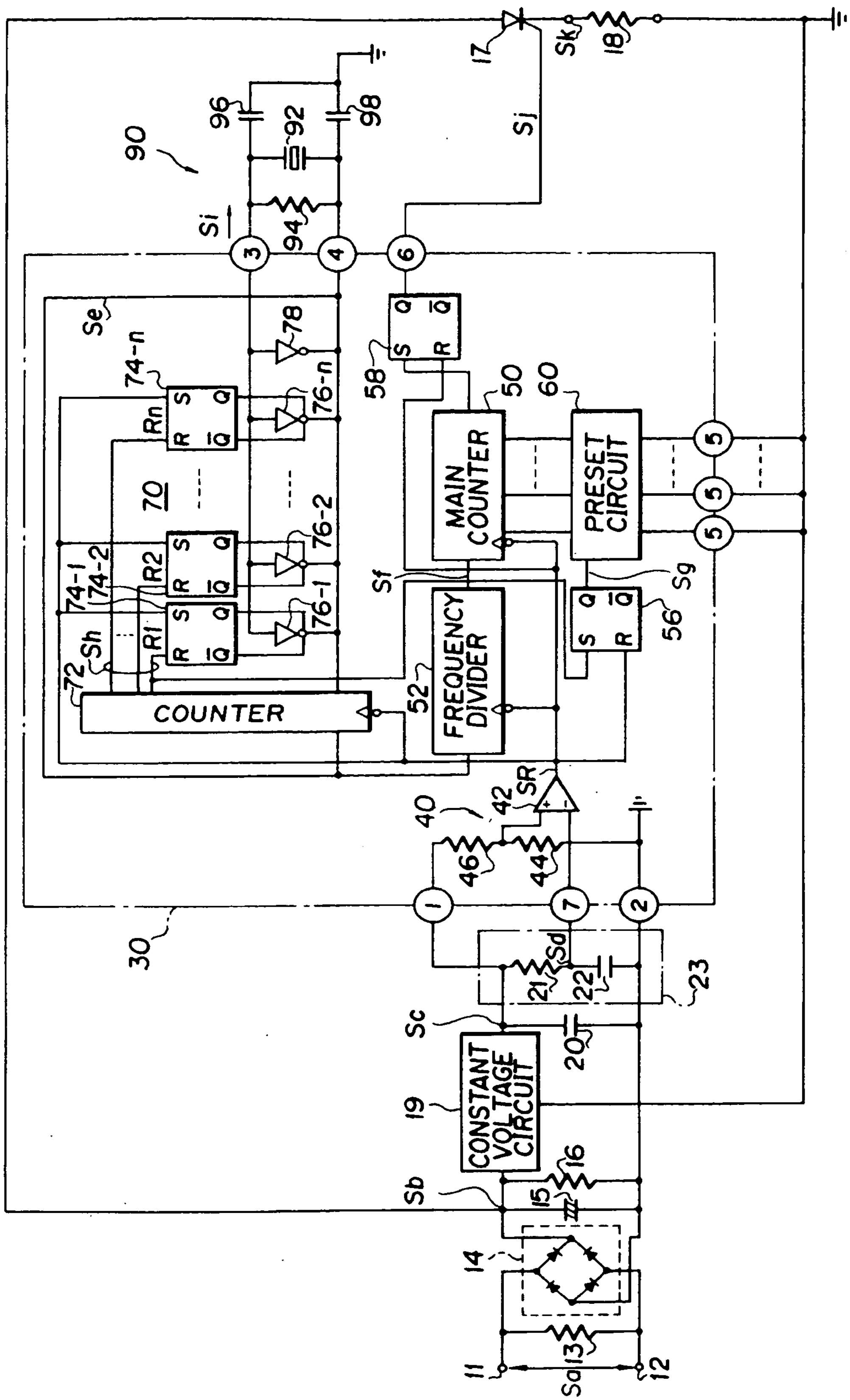
CONSTANT VOLTAGE CIRCUIT
FREQUENCY DIVIDER
MAIN COUNTER
PRESET CIRCUIT
COUNTER

FIG.3

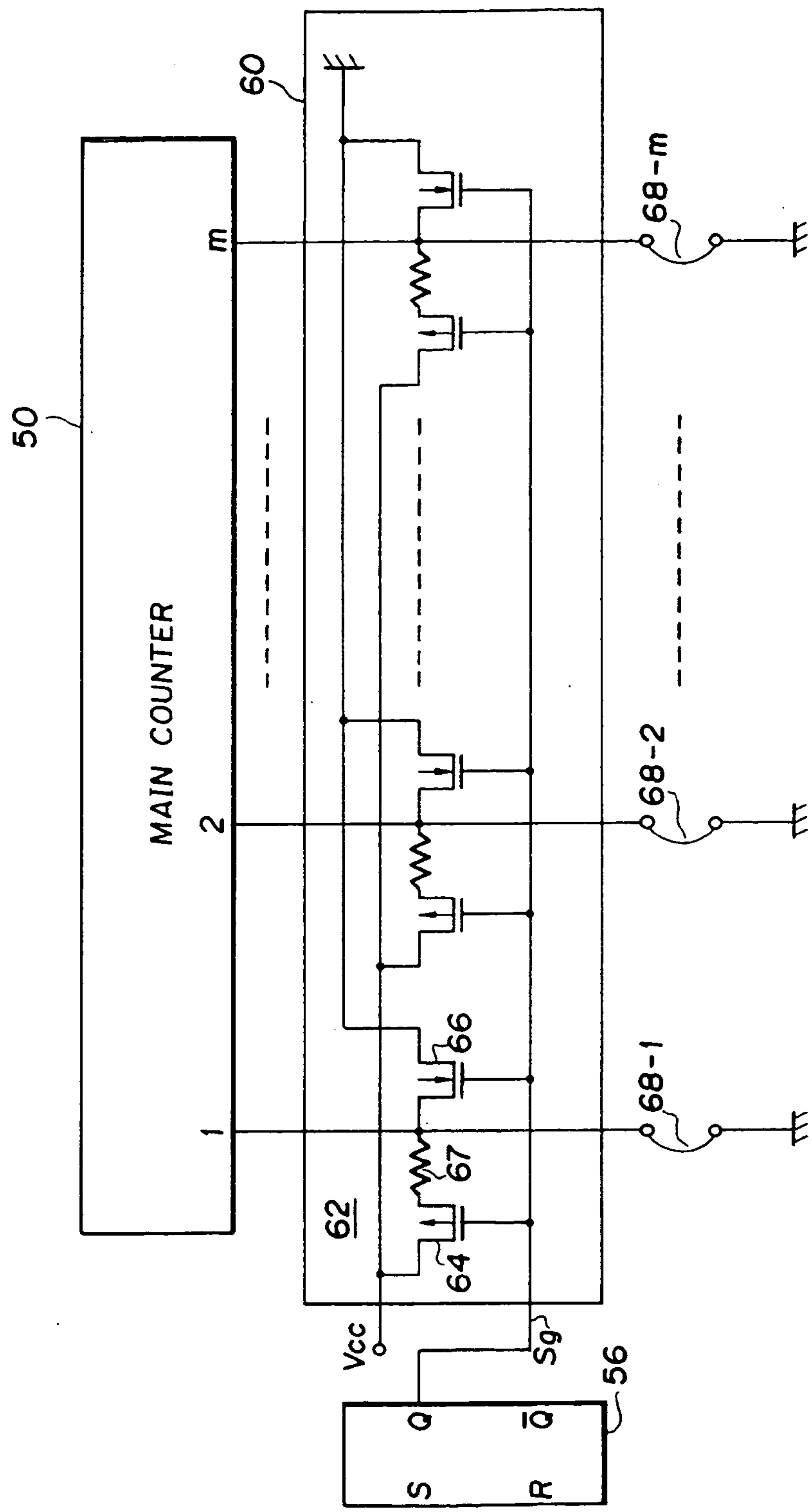
MAIN COUNTER
50
60
62
64
66
67
1
2
m
68-1
68-2
68-m
Vcc
Sg
56
Q
$\overline{Q}$
S
R

FIG. 4A

76-i

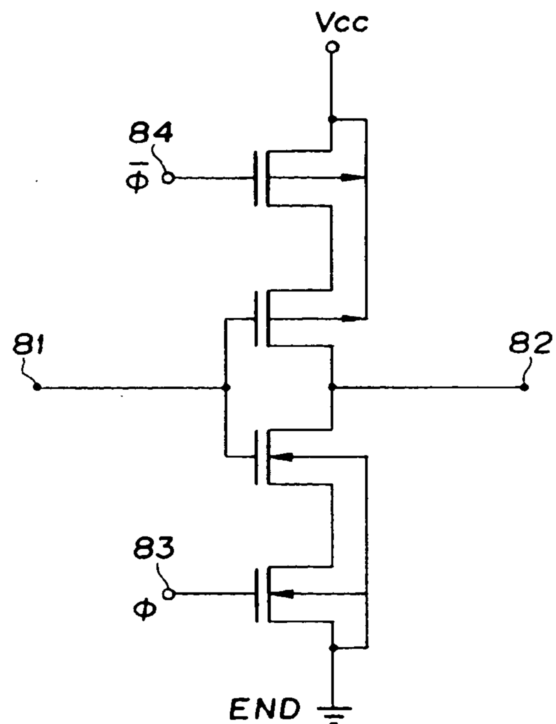

FIG.4B

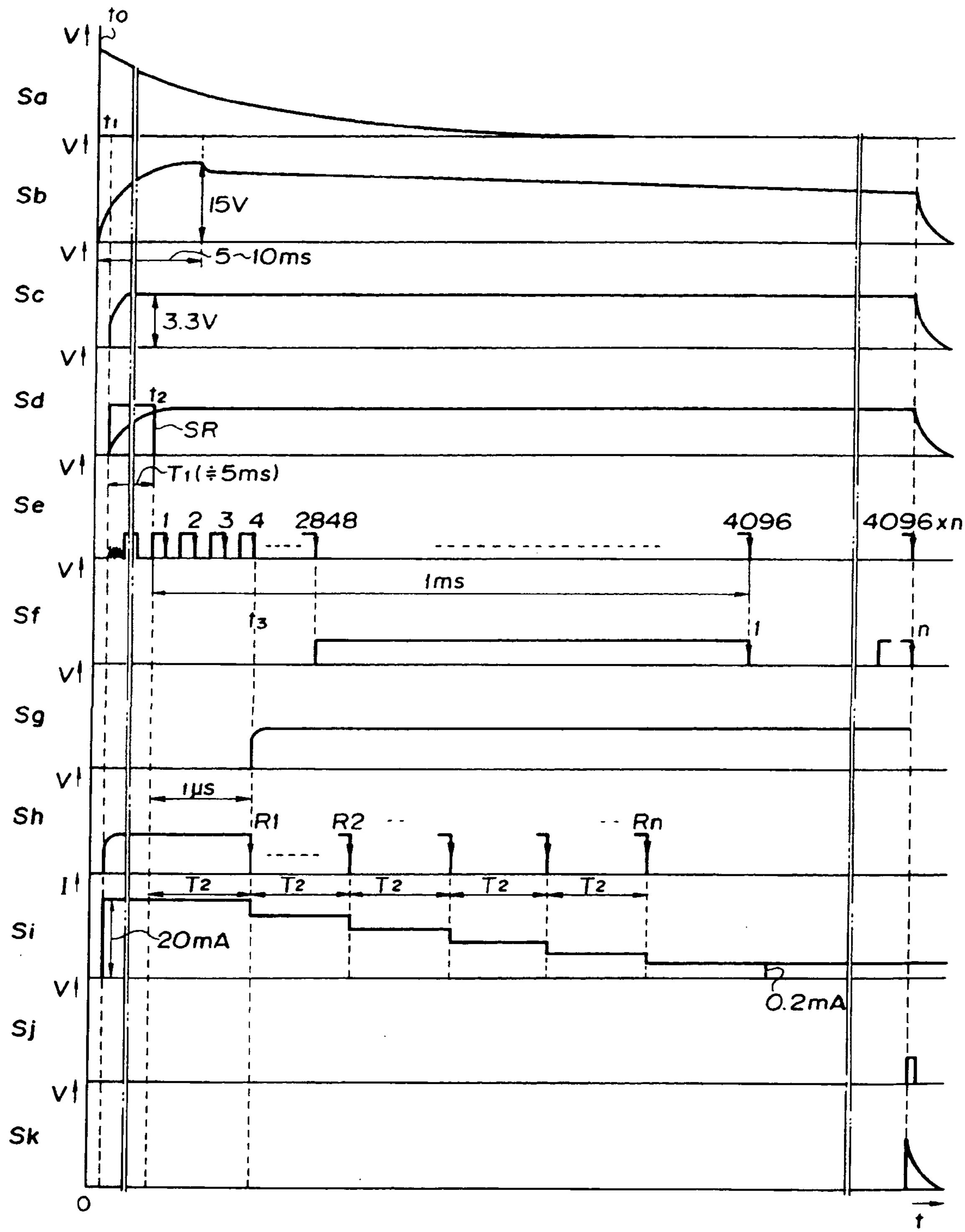
t0
Sa
t1
Sb
15V
5~10ms
Sc
3.3V
Sd
t2
SR
Se
T1(≒5ms)
1 2 3 4 2848 4096 4096xn
Sf
1ms
t3
1
n
Sg
Sh
1μs
R1 R2 Rn
Si
T2 T2 T2 T2 T2
20mA
0.2mA
Sj
Sk
0
t

FIG.5

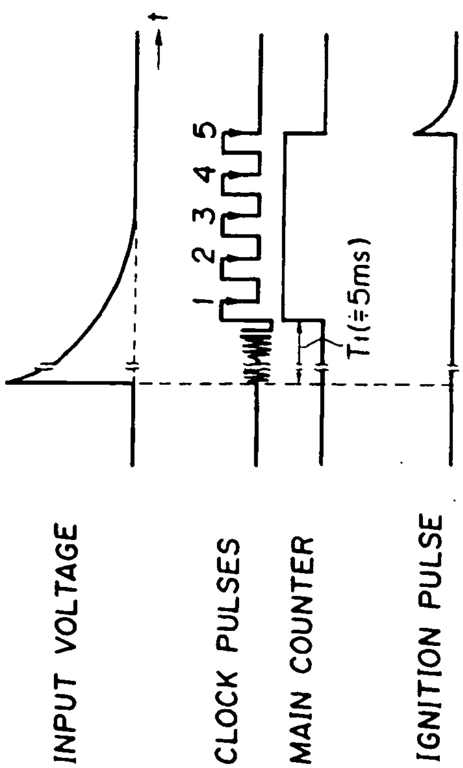

FIG.6A

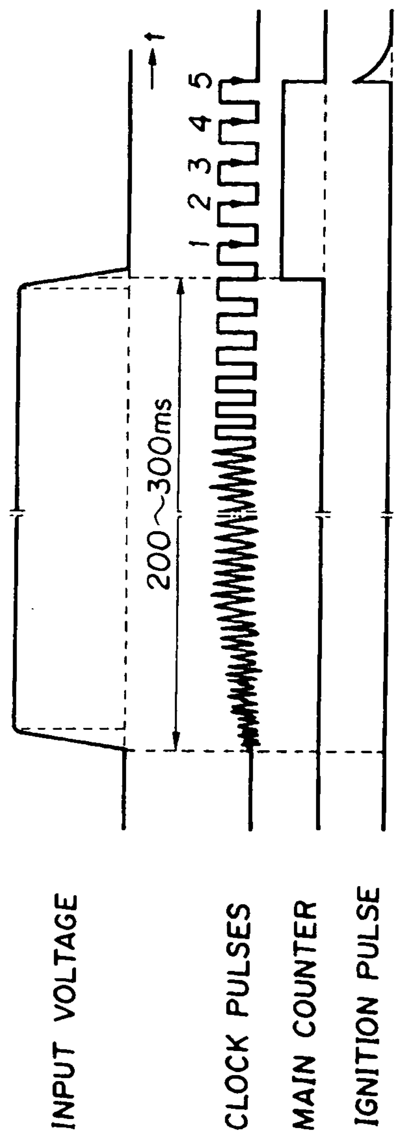

FIG.6B PRIOR ART

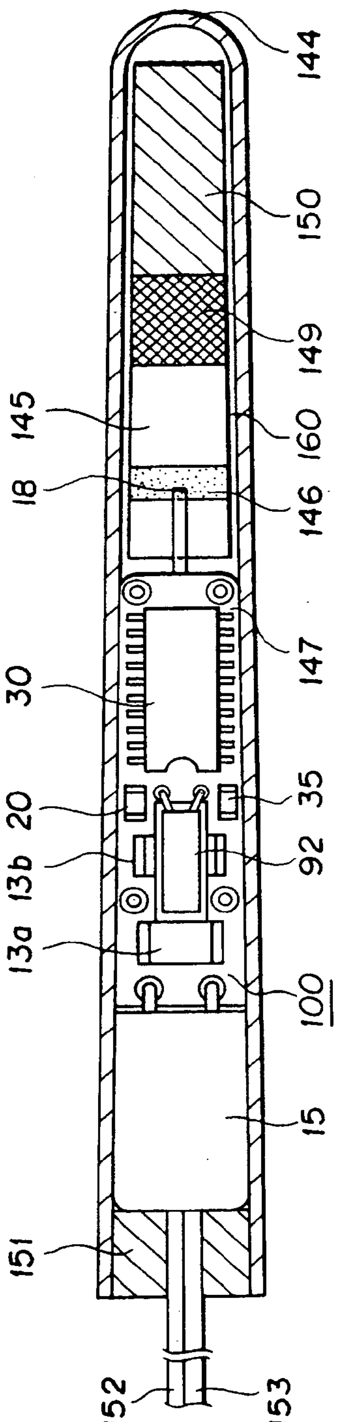
144
150
149
145
160
18
146
147
30
20
35
13b
92
13a
100
15
151
152
153

FIG.7

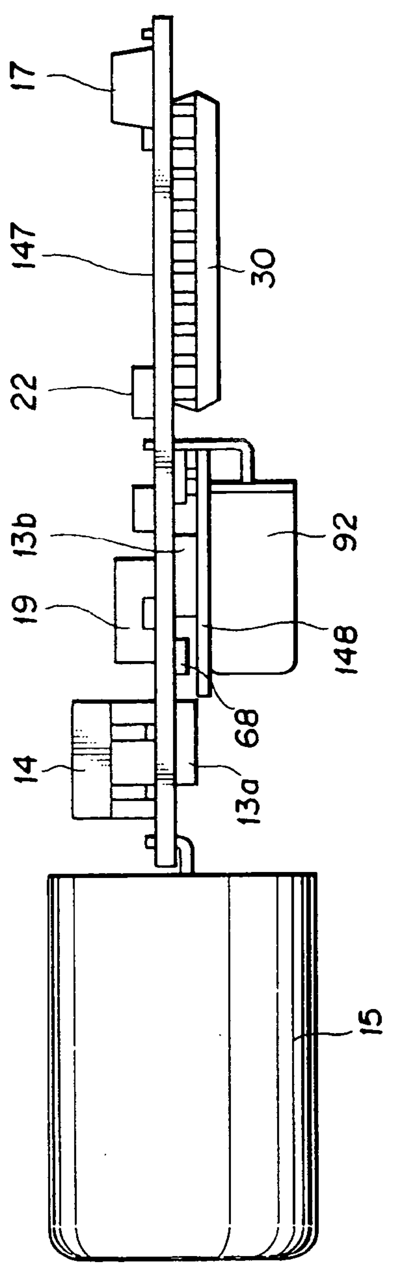

FIG.8A

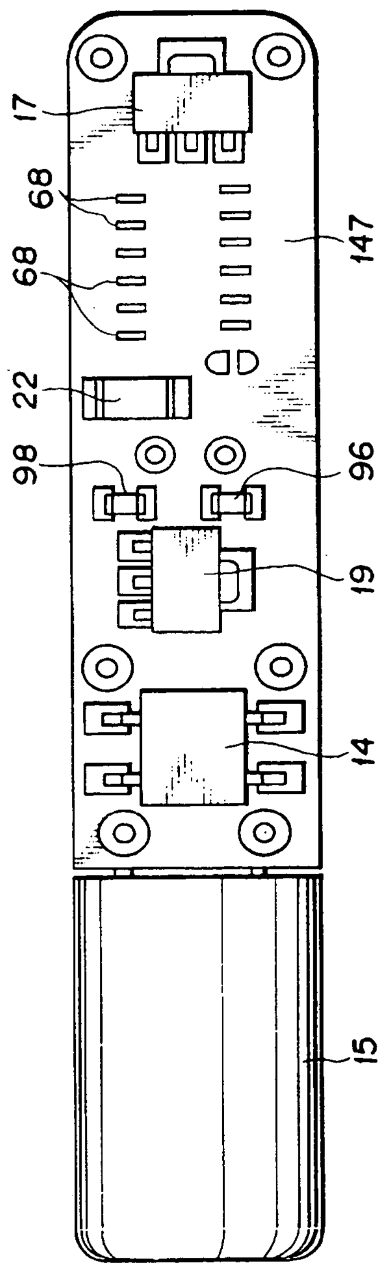

FIG.8B

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 93 10 4305

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
Y,D	US-A-4 445 435 (OSWALD) * column 3, line 6 - line 23 * * column 6, line 11 - line 65 * * column 8, line 46 - column 10, line 9 * * figures * ---	1-4,6,7, 16-18,25	F42D1/055 H03L3/00
Y	US-A-5 041 802 (WEI ET AL.) * column 1, line 46 - line 68 * * figures * ---	1-4,6,7, 16-18,25	
A	US-A-5 117 756 (GOFFIN, II) * column 2, line 35 - column 3, line 2 * * figures * ---	1,16,25	
A	US-A-4 560 954 (LEACH) * column 3, line 3 - line 33 * * figures * ---	1,16,25	
A,D	EP-A-0 386 860 (NIPPON OIL AND FATS COMPANY, LIMITED) * column 2, line 12 - column 3, line 36 * * figures * -----	1,16,25	TECHNICAL FIELDS SEARCHED (Int. Cl.5) F42D H03L F42C F42B H03B H03K

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	23 AUGUST 1993	OLSSON B.G.

CATEGORY OF CITED DOCUMENTS

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P : intermediate document

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E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document